

AREA ARRAY TECHNOLOGY EVALUATION FOR SPACE AND MILITARY APPLICATIONS

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ABSTRACT

The Jet Propulsion Laboratory (JPL) is currently assessing the use of Area Array Packaging (AAP) for National Aeronautics and Space Administration (NASA) spaceflight applications. This work is being funded through NASA Headquarters, Code Q. The objectives of the project are to demonstrate the robustness, quality and reliability of AAP technology, and to assist in the development of the rapidly growing industrial infrastructure for this technology. JPL has solicited industrial, academic and other related consortia to work together to leverage the related efforts into a synergistic cooperative effort. All participants in this effort are furnishing in-kind contributions. The wide industrial use of AAP technology will afford NASA as well as consortium industries inexpensive access to this technology and support miniaturization thrusts for their next generation applications.

The Consortium will characterize AAPs (often referred as Ball Grid Arrays, or BGAs) in the following areas:

- Processing/assembling Printed Wiring Boards (PWBs) using AAPs, including rework
- Inspection and Quality Assurance (QA) methods for ascertaining the process controls, acceptance methodologies and final quality of AAP assemblies.
- Investigating the reliability of assemblies utilizing AAPs in several different types of environments (thermal and dynamic).

Parameters inside the design, manufacturing and test of the test vehicles are being statistically toggled using a Design of Experiment (DoE) technique to determine the influence and criticality of these parameters. The status of this effort is presented.

** Names of consortium team members are listed in the acknowledgment.*

BACKGROUND

The production of surface mount assemblies (SMAs) now surpasses assemblies using through hole technology (THT). In surface mount technology (SMT), components are mounted and terminated directly onto the printed wiring board (PWB) surface. One of the most important component parameters is the lead pitch, which is continuously decreasing to meet the need for higher I/O count.

The use of fine and ultra fine pitch (FP and UFP) components with less than 0.020 inch pitch is growing, often resulting in more than 200 leads for a single device. Typically, these components have gull wing leads. FP and UFP components, in addition to being extremely delicate and easily damaged during handling, are also difficult to process and are prone to misalignment, and rework with the associated reliability implications.

One important emerging technology for utilizing higher pin counts, without the attendant handling and processing problems of the peripheral array packages (PAP), is AAP. Unlike PAPs, AAPs have pins, or terminations, covering the entire area, or a large portion of the area, on the bottom of the package.

AAPs offer several distinct advantages over FP and UFP SMCS having gull wing leads, including:

- AAPs are capable of high pin counts, generally > 200 (easily above 500 I/O).
- Larger lead pitches, which significantly reduces the manufacturing complexities for high I/O parts.
- Higher packaging densities are achievable since the lead envelope for the gull wing leads is not applicable in the case of AAPs; hence, it is possible to mount more packages per board.
- Faster circuitry speed than gull wing SMCS because the terminations are much shorter.
- Better heat dissipation than gull wing lead SMCs.

The AAPs are also robust in processing. This stems from their higher pitch (0.050 inch typical), better lead rigidity, and self-alignment characteristics during reflow processing.

AAPs, however, are not compatible with multiple solder processing methods and individual solder joints cannot be inspected and reworked using conventional methods. In ultra low volume SMT assembly applications, e.g., NASA's, the ability to inspect the solder joints visually has been standard and is a key factor providing confidence in the solder joint reliability.

OBJECTIVES

The objectives of consortium efforts are to demonstrate the robustness, quality and reliability of AAP technology for space and military applications and to further infrastructure development for this technology. The organizations that are involved to-date include:

- **Military sectors-** Hughes Missile Systems Company (HMSC) to design Printed Wiring Board (PWB), Boeing Defense and Space Group to perform environmental testing for military applications, and Loral, Canada, to test and validate the reliability of test vehicles assembled in a military manufacturing facility.
- **Commercial facilities-** Amkor/Anam Electronics, Inc.. to provide plastic packages, Altron Inc. to fabricate PWBs, Celestica, Canada, to assemble test vehicles, Electronics Manufacturing Productivity Facility (EMPF) to perform environmental testing, American Micro Devices (AMD) to provide resistive die, IBM to provide ceramic packages, Nicolet for X-ray, and View Engineering to measure coplanarity and warpage of packages using their 3-D laser scanning equipment.
- **Infrastructure-** Interconnection Technology Research Institute (ITRI) established by the Institute for Interconnecting and Packaging Electronic Circuits (IPC) to provide a vehicle for collaboration among the various sectors of electronic interconnection industries.
- **Academia-** Rochester Institute of Technology (RIT) to assemble test vehicles. More than 20 industrial advisors including people from JPL helping to redirect the RIT metal manufacturing laboratory into a Computer Integrated Electronics Manufacturing (CIEM) facility to help meet the current national demand for electronics manufacturing engineers.

The DoE test matrices, a combination of full and fractional factorials, have gone through several revisions to meet the objectives of the programs and to satisfy team members' needs. Currently, a minimum of 200 test vehicles will be required to meet the test plan. This does not include additional test vehicles to be assembled at Loral/Canada, a recent additional participant in the project,

Test vehicles are manufactured at three sites, a commercial facility with extensive experience, a military facility with some experience, and a university with minimum experience in assembling BGAs. Assemblies will be subjected to various types of inspection including X-ray and scanning electron microscopy before and during environmental exposure. During environmental exposure, test vehicles will be monitored continuously through a daisy chain and will be removed periodically and cross-sectioned for crack propagation mapping.

Data collected will be analyzed and categorized using the Weibull distribution, and the Coffin-Manson relationship for the cycles to failure distribution and failure projection. Manufacturing defect and occurrence frequencies for different surface finishes and package types and configurations will be correlated. Modeling techniques will be used to correlate theory and the experiment. The output of this effort will be published in a suitable industrial guidelines document, providing a common point of reference and use between NASA/JPL and industry for this technology.

TEST MATRIX VARIABLE IDENTIFICATION

Test matrix variables were discussed in numerous telecons among the consortium core members. A workshop was held at JPL in March 1994 to narrow the test matrix definition, teaming arrangement, and level of participation of consortia members. Attendees were core members (JPL, Hughes, RIT, and Boeing), and ITRI, SEMATECH, and EMPF. In the workshop, participants presented issues related to the BGA technology, their areas of interest, and provided further insight towards implementation of a suitable test vehicle. These are summarized below.

JPL's focus is to establish and define high reliability inspection methodologies for AAPs. This includes a comparison of both the plastic and ceramic BGAs' reliability performance in different environments. JPL will establish manufacturing parameters, boundaries and controls, for ultra-low volume applications and will coordinate cooperation with industry for developing suitable design guidelines for AAPs/BGAs.

JPL is involved in several ARPA funded projects on interconnect technology. One is "Low Cost Packaging Through a Systems Approach To Ball Grid Array Package Assembly" which was funded by ARPA to the Ultra Clean International Corp. (UCIC). The objective of the UCIC program is to develop a lower cost and more environmentally friendly approach to assembling Ball Grid Array (BGA) packages. BGA packages are expected to become the predominant form factor for high pin-count devices used in both military and commercial applications.

Hughes (HMSC) major products are missile systems with no missile program currently utilizing BOA technology. Because of space constraints in board designs, BGAs have become an attractive alternative replacing quad flatpack (QFP) devices. Hughes' objectives are to rapidly adopt this technology in their programs such as RAM and Stinger. Cost and space

saving are the motives, and their objectives will be aided by industry and program leveraging.

RIT is primarily a technology university concentrating on engineering applied research. The microelectronics facility is available for fabrication of chips and also component assembly of printed wiring boards. They have advanced expertise in computer engineering technology, information technology, and close ties to the electronic industry.

The RIT manufacturing laboratory was focusing on metal manufacturing, but this was redirected to meet national demand for electronic manufacturing engineers. More than 20 industrial advisors including JPL are involved in many aspects of the laboratory including definition of the scope of the curriculum, needs of industry, laboratory resources, and analysis of long term trends in technology.

Boeing is interested in obtaining reliability data on BGA assemblies from a users' point of view. They are also interested in participating in standardization of BGA parts. Potential areas for Boeing participation are:

- Reliability testing such as thermal cycling
- Board level assembly process evaluation and materials characterization
- Test vehicle design, DoE
- Part standardization and technical specification development

ITRI was created in 1994. ITRI is sponsored by the IJC. ITRI's primary focus is on PWBs and PWAs and like SEMATECH and unlike MCC (Micro Computer Technology Corporation), is a virtual consortium. That is, it does no research on its own; for it has neither facilities nor personnel by which to accomplish this. Rather, its objective is to define and guide necessary research projects to make the US interconnect/packaging industry economically more competitive. ITRI guides and directs R&D projects among its participating members by periodically bringing members together to discuss results, receive feedback at review meetings, and plan future activities.

ITRI at the time of this writing was working in six areas, two government funded environmental effects studies and TRPs. Three of the projects are in the implementation phase while the other three are in the definition phase. The project "Implementation of Organic Solder Preservative (OSP), alternative platings for elimination of Hot Air Solder Leveling (HASL)" was presented. OSP is becoming the choice of surface finish and therefore majority of test vehicle will be OSP coated.

Viewgraphs that showed the relationship between pin count and cost/performance were presented. It was apparent that peripheral leads will soon fall short of meeting advanced packaging requirements. However, for BGAs there are a wide range of I/O, pitch, and sizes meeting both a near term demand and future long term requirements. Cost/performance requirements for QFPs to meet near term future requirements are even more disparate.

SEMATECH has been in business for six years and its goal is to solve the technical challenges required to keep the US number one in the global semiconductor industry. Several programs, mostly semiconductor fabrication, have been identified that address the need of its members. The assembly and packaging has been added recently and its mission is to provide the competitive assembly and advance packaging manufacturing technologies necessary to enable SEMATECH member companies and the supporting domestic infrastructure to compete effectively in global markets.

In reviewing packaging technology trends, SEMATECH forecast different types of electronic packages for surface mount applications. These include plastic quad flat pack (QFP), plastic ball grid array (PBGA), ceramic ball grid array (CBGA), and thin tape carrier package (TCCP). Comparison of low, medium and high I/O counts were presented. There are QFP packages in the medium range while at high I/O count only BGAs and TCPS are cost/performance competitive, but not QFPs.

SEMATECH is also involved in BGA technology development and its aim is to provide the needed infrastructure for meeting the accelerated transition to BGA technology. The specific needs range from a low-cost package substrate to inspection equipment and reliability data. Currently, about 60% of laminate structures use PBGA for low cost, but CBGA is used if reliability/performance is the chief requirement criterion. Some work on μ BGA is on the horizon, but member companies will become more interested when the cost trade off is shown.

EMPF was funded by the National for Excellence about 10 years ago to develop and capture manufacturing technologies that were rapidly exiting the US. They have chiefly focused their efforts on the effects of assembly and rework on reliability, and the correlation of inspection results to reliability. The EMPF began investigating manufacturing and related issues of BGAs in 1993. They have experience mainly with plastic OMPAC type BGA components and FR-4 PWBs. They are willing to expand their involvement with ITRI and are able to perform manufacturing and in-process inspection utilizing a Four Pi X-ray system.

After presentations, many issues were discussed regarding the selection of test matrix parameters for the investigation. Issues discussed are:

- Need to further define the test vehicle based on the objectives and need of industry.
- Pretesting might be needed before evaluation for test vehicle optimization,
- Need to leverage from the work performed by others. Enough data are available that many manufacturing variables don't have to be considered.
- SEMATECH project data on cost/performance need to be used to better define test vehicles.
- Delco has performed a study on BGAs and QFPs. Need to understand what they have done.
- Standard practices or as close to them as possible need to be used for the test vehicle design and the manufacturing variables.
- Use the JEDEC standard for pitch size. There are no standards on many issues. IBM and Motorola have their own standards.
- Coordinate activities with the IJC.
- FR-4 was ranked high and then polyimide. FR-4 is widely used and also larger differences in Coefficient of Thermal Expansion (CTE) with BGAs compare to polyimide will provide the most conservative reliability test results.
- The 3001/OBGAs are considered soon to be norm where BGAs compete with leaded packages and 600 I/O are for the near future in BGA packages. Both plastic BGA and ceramic BGA packages need to be evaluated.
- No interest at this time in evaluation of column ball grid array.
- We need to evaluate both full array and peripheral array because of concern about the reliability of solder joints under die.
- Characterization of solder paste is important.
- Solderability is important and must be evaluated. At the package level solderability is OK but at the assembly level solderability needs to be tested.
- It is very important to use die even though it is costly.
- Underfilling is generally done to promote the thermal enhancement and vibration tolerance but not reliability.
- Regarding power cycling, resistive die will be used.
- The JPL study indicated the importance of vibration and mechanical shock. The effect of vibration needs to be investigated further.
- Only edge balls can be detected visually and by SEM. The best way to monitor crack initiation and propagation needs to be defined.
- JPL uses Anatech® to continuously monitor for electrical opens. Cross-sectioning, also can be done.

- It is the ball height after reflow, rather than the ball size that affects solder joint reliability.
- Solder volume is more critical for some types of package than others. It is important to include solder volume as a variable in the DOE test program,
- Surface finish plating, i.e., hot air leveling (HASL), or use of organic solder preservative (OSP) are important and should be considered.
- Solder mask has shown to be a factor affecting reliability.
- Need to look into underfilling.
- Need to look into conformal coating.

Subsequent to the Workshop and after extensive discussion and further ranking of variables discussed, the following most critical issues were determined:

- Determine a suitable inspection technique for AAP/BGA packages, particularly after they have been attached to the substrate.
- Decide on the optimal package type array configuration: peripheral array versus full area array package and assess the reliability performance of each array type.
- Characterize the reliability differences between ceramic and plastic BGAs.
- Assess the various techniques for reworking AAP/BGA packages.

DOE TEST MATRIX

It would be desirable to define a test matrix that could successfully resolve most of the above issues and provide statistically significant results. Statistical significance could be further increased by use of duplicates for each variable. An alternative to testing one variable at a time is DoE. Full factorial experiments require the maximum number of test vehicles compared to fractional factorials, but they also provide more statistically meaningful data. Fractional factorials allow the maximum statistical return with a minimum test matrix.

The DoE test matrix has been revised several times to meet the objectives of the program and to include new team members' needs. Currently, a minimum of 200 test vehicles will be required to meet the test plan, cost, facility capability for board fabrication and assembly, and the availability of environmental chambers are the primary reasons for the experiment limitations. This does not include additional test vehicles to be assembled at Loral/Canada, a recently joined consortium member.

Table 1 illustrates the current DoE test matrix that the consortium team is focusing their activities on. This

includes two board designs, two thermal cycle profiles, and a combination of thermal and mechanical environmental exposure. Power cycling will be performed using 560 Super BGA with AMD resistive die to better understand the behavior in a more realistic environment.

Two types of board material, polyimide and FR-4 and eight types of packages were used. Full array ceramic and plastic and plastic peripheral array packages were used. The BGA parts selected have I/O counts of approximately 300 and 600. The 256 FPQF, 0.4 inch pitch, was included to evaluate manufacturing challenges associated with mixed technology as well as to directly compare the reliability of 256 lead FPQF and BGA assemblies. Three levels of solder volume (standard, low, and high) will be toggled with I/O counts, PWBs, and package types to fully characterize the effects of solder volume. Three types of surface finishes with emphasis on OSP will be used. Two flux types, RMA and water soluble, with emphasis on RMA, will be characterized. Two manufacturing sites, mature; Celestica, and start up, RIT, are considered for assembling.

The rationale for selection and toggling of the DoI parameters, test vehicle configuration, environmental testing, and quality assurance methodologies follow. Information includes mostly those that are currently established and agreed on by the team members.

PWB MATERIALS AND PACKAGES

Figure 1 shows the test vehicle configuration. Two types of board materials, polyimide and FR-4 and eight package types were used.

The FR-4 PWB represents the most commonly used resin system material. The glass transition temperature (T_g), that is, the transition from a rigid to a rubbery material, of FR-4 ranges from 130° to 180°C, depending on the functionality of the epoxy. This is sufficient for most commercial and some military applications. Higher glass temperature polyimide (T_g over 200°C) resin material is commonly used for higher temperature applications.

Two package types, plastic and ceramic, are being considered for evaluation. There are technical concerns about the use of plastic packages. However, their low cost and availability in numerous different I/O counts (< 400) make them extremely attractive for space and military applications. The tests that will be conducted are defined so as to identify some of the limitations that are associated with the use of plastic packages. On the other hand, ceramic packages have been used in most military/space

applications. They are especially attractive at high I/O counts.

The I/O count was selected based on the current and future market trend forecast presented by SEMATECH at the JPL Workshop. BGAs with I/O counts of over 300 become cost/performance competitive compared to QFPs. With the rapid increase and demand for higher I/O counts, it is anticipated that soon an I/O count greater than 600 will be the norm.

Also, two types of array populations i.e. full and peripheral will be evaluated. Peripheral array, especially for plastic packages, has been developed to increase reliability as well as to ease routing. Removal of the center solder balls, however, will slightly degrade thermal performance (θ_{ja}) of these packages. Addition of a small number of solder balls in the middle of package's ground plane are used to improve the thermal performance.

For plastic packaging, the importance of die size on solder joint performance is well established. Experimental results indicate that solder joints close to the perimeters of the die fail first under temperature cycling. The cycle-to-failure has shown that cycle to failure does not follow the I/O count, but rather the die size. The CTE between a ceramic die (2.3 ppm/°C) and an encapsulated epoxy (15 ppm/°C) is the key contributing factor. Peripheral packages were developed to reduce solder joint failure at the die edge as well as improve routing characteristics. For the ceramic package, because the CTE mismatch is negligible, there is a lesser need for a peripheral package design.

Table 2 lists package types with I/O count, source of package manufacturer, and resistive or dummy die sizes that will be used for evaluation. Note that for the plastic packages, both peripheral and full array are available and will be tested. For ceramic packages, only the full array version will be used. The 352 Over Molded Pad Array Carrier (OMPAC) will be directly compared to a 352 Super BGA (SPBGA). Reliability of a 256 PBGA will be compared to a conventional fine pitch gull wing package.

Lay-out Design Issues

Figure 2 shows the board lay-out for type 1, "300" I/O count, and type 2, "600", configurations. Some of the design features are:

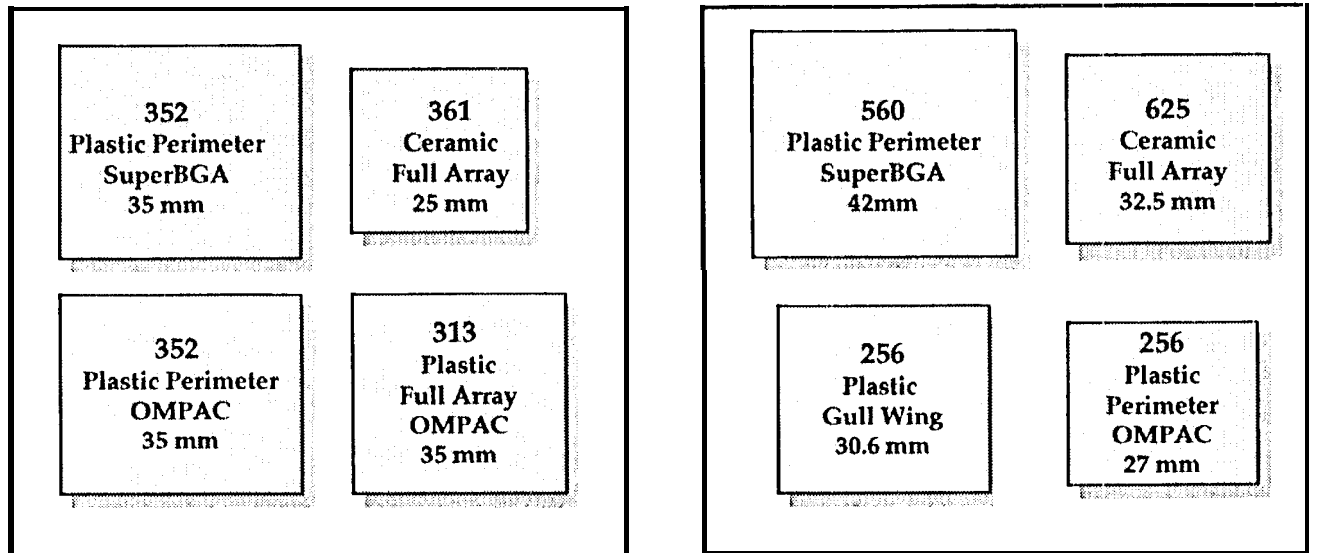
- PWBs were designed such that each package is independent and could be cut for failure analysis and evaluation immediately after failure detection.
- Packages were daisy chained for electrically monitoring solder joint failures during environment exposure. A typical daisy chain has four regions: outer edges, beneath the die, die edges, and between

TABLE 1. DoE 1 EST Matrix

| TABLE 1. DoE 1 EST Matrix | | | | | | | | | | |
|---------------------------|-----------|-----------|---------------|------------|----------------|-----------|-------------------|--------------|------------|---------------|
| # | PWB | I/O | Solder Volume | Paste Flux | Surface Finish | Assembler | Power Chip 5601/0 | Cycling Site | Replicates | Cross section |
| 1 | FR-4 | "300" I/O | Nominal | RMA | OSP | Cel | No | Boeing | 5 | 2 |
| 2 | Polyimide | "300" I/O | Nominal | RMA | OSP | Cel | No | Boeing | 6 | |
| 3 | FR-4 | "600" I/O | Nominal | RMA | OSP | Cel | No | Boeing | 4 | |
| 4 | Polyimide | "600" I/O | Nominal | RMA | OSP | Cel | No | Boeing | 4 | |
| 5 | FR-4 | "300" I/O | Nominal | RMA | OSP | Cel | No | "EMPF | 5 | 2 |
| 6 | Polyimide | "300" I/O | Nominal | RMA | OSP | Cel | No | EMPF | 7 | |
| 7 | FR-4 | "600" I/O | Nominal | RMA | OSP | Cel | No | EMPF | 5 | |
| 8 | Polyimide | "600" I/O | Nominal | RMA | OSP | Cel | No | EMPF | 5 | |
| 9 | FR-4 | "300" I/O | Nominal | W soluble | OSP | Cel | No | EMPF | 5 | 3 |
| 10 | Polyimide | "300" I/O | Nominal | W soluble | OSP | Cel | No | EMPF | 3 | |
| 11 | FR-4 | "600" I/O | Nominal | W soluble | OSP | Cel | No | EMPF | 3 | |
| 12 | Polyimide | "600" I/O | Nominal | W soluble | OSP | Cel | No | EMPF | 3 | |
| 13 | FR-4 | "300" I/O | Nominal | RMA | OSP | Cel | No | JPL | 5 | 3 |
| 14 | Polyimide | "300" I/O | Nominal | RMA | OSP | Cel | No | JPL | 8 | |
| 15 | FR-4 | "600" I/O | Nominal | RMA | OSP | Cel | No | JPL | 4 | |
| 16 | Polyimide | "600" I/O | Nominal | RMA | OSP | Cel | No | JPL | 8 | |
| 17 | FR-4 | "300" I/O | Nominal | W soluble | OSP | Cel | No | JPL | 5 | 2 |
| 18 | Polyimide | "300" I/O | Nominal | W soluble | OSP | Cel | No | JPL | 5 | |
| 19 | FR-4 | "600" I/O | Nominal | W soluble | OSP | Cel | No | JPL | 3 | |
| 20 | Polyimide | "600" I/O | Nominal | W soluble | OSP | Cel | No | JPL | 0 | |
| 21 | FR-4 | "300" I/O | Nominal | RMA | OSP | RIT | No | JPL | 5 | 2 |
| 22 | Polyimide | "300" I/O | Nominal | RMA | OSP | RIT | No | JPL | 7 | |
| 23 | FR-4 | "600" I/O | Nominal | RMA | OSP | RIT | No | JPL | 4 | |
| 24 | Polyimide | "600" I/O | Nominal | RMA | OSP | RIT | No | JPL | 4 | |
| 25 | FR-4 | "300" I/O | Low | RMA | OSP | RIT | No | JPL | 5 | 3 |
| 26 | Polyimide | "300" I/O | Low | RMA | OSP | RIT | No | JPL | 0 | |
| 27 | FR-4 | "600" I/O | Low | RMA | OSP | RIT | No | JPL | 0 | |
| 28 | Polyimide | "600" I/O | Low | RMA | OSP | RIT | No | JPL | 0 | |
| 29 | FR-4 | "300" I/O | High | RMA | OSP | RIT | No | JPL | 0 | 3 |
| 30 | Polyimide | "300" I/O | High | RMA | OSP | RIT | No | JPL | 0 | |
| 31 | FR-4 | "600" I/O | High | RMA | OSP | RIT | No | JPL | 3 | |
| 32 | Polyimide | "600" I/O | High | RMA | OSP | RIT | No | JPL | 0 | |
| 33 | FR-4 | "300" I/O | Low | RMA | OSP | Cel | No | JPL | 5 | 3 |
| 34 | Polyimide | "300" I/O | Low | RMA | OSP | Cel | No | JPL | 3 | |
| 35 | FR-4 | "600" I/O | Low | RMA | OSP | Cel | No | JPL | 3 | |
| 36 | Polyimide | "600" I/O | Low | RMA | OSP | Cel | No | JPL | 3 | |
| 37 | FR-4 | "300" I/O | High | RMA | OSP | Cel | No | JPL | 3 | 3 |
| 38 | Polyimide | "300" I/O | High | RMA | OSP | Cel | No | JPL | 3 | |
| 39 | FR-4 | "600" I/O | High | RMA | OSP | Cel | No | JPL | 3 | |
| 40 | Polyimide | "600" I/O | High | RMA | OSP | Cel | No | JPL | 3 | |
| 41 | FR-4 | "600" I/O | Nominal | RMA | HASL | Cel | YES | JPL | 0 | 3 |
| 42 | Polyimide | "600" I/O | Nominal | RMA | HASL | Cel | YES | JPL | 5 | |
| 43 | FR-4 | "600" I/O | Nominal | RMA | Ni/Au | Cel | YES | JPL | 7 | |
| 44 | Polyimide | "600" I/O | Nominal | RMA | Ni/Au | Cel | YES | JPL | 7 | |
| 45 | FR-4 | "600" I/O | Nominal | RMA | OSP | Cel | YES | JPL | 10 | 3 |
| 46 | Polyimide | "600" I/O | Nominal | RMA | OSP | Cel | YES | JPL | 10 | |
| 47 | Polyimide | "300" I/O | Nominal | RMA | OSP | Cel | Vibrator | JPL | 7 | |
| 48 | FR-4 | "300" I/O | Nominal | RMA | OSP | Cel | Vibrator | JPL | 7 | |
| Total | | | | | | | | | 197 | |

TABLE 2. Test Vehicle Package Data

| Board Type | PKG ID | Part Type | I/O | Materials Configurations | Source | Size (mm sq) | Wiring | Pitch | Selected Die Size | Die Cavity | Die Range |
|------------|--------|------------|-----|--|---------|--------------|----------|-------|-------------------|---------------|------------|
| 1 | 1 | *PBGA 300' | 352 | Plastic/peripheral/ SUPER BGA | Amkor | 35 | No daisy | 1.27 | 13.3 | 14.3/15.6 | 11.44-14.6 |
| 1 | 2 | "PBGA 300' | 352 | Plastic/Peripheral/ OMPAC | Amkor | 35 | Daisy | 1.27 | 13.3 | 7.5, 8.5, 9.5 | 7.5-9.5 |
| 1 | 3 | *CBGA 300' | 361 | Ceramic/Full array Plastic/Full array/ OMPAC | IBM | 25 | Daisy | 1.27 | 13.3 | 9.5 | 8.5-9 |
| 1 | 4 | *PBGA 300' | 313 | Plastic/Peripheral/ SUPER BGA | Amkor | 35 | Daisy | 1.27 | 15.25 | 7.5 std | 15.4-17.3 |
| 2 | 5 | *PBGA600" | 560 | Ceramic/Full array | Amkor | 42 | Daisy | 1.27 | 10.8 | | 6.5-8.5 |
| 2 | 6 | *CBGA600" | 625 | Plastic/Peripheral | IBM | 32.5 | No Daisy | 1.27 | | | |
| 2 | 7 | *PBGA 300' | 256 | Plastic/Gull wing | Amkor | 27 | Daisy | 0.4 | | | |
| 2 | 8 | *GW" | 256 | | TOPLINE | 30.6 | | | | | |



Type 1 "300" 1/0s

Type 2 "600" 1/0s

Figure 1. Board Lay-Out for Type 1 and Type 2 Test Vehicles

TABLE 3. Laser Scanning Planarity Data

| Package ID | Package Type | Coplanarity Max. (roils) | Coplanarity Min. (mils) | Ball Width Min. (mils) | Bali Width Max. (roils) | Bali Width Avg. (roils) |
|------------|--------------|--------------------------|-------------------------|------------------------|-------------------------|-------------------------|
| 2 | CBGA625 | 2.9 | 0.78 | 33.92 | 36.67 | 34.88 |
| 3 | CBGA625 | 2.41 | 0.77 | 33.88 | 36.28 | 34.79 |
| 2 0 1 | CBGA 361 | 2.18 | 1.04 | 34.11 | 37.35 | 35.14 |
| 202 | CBGA 361 | 2.49 | 0.92 | 33.73 | 36.41 | 34.59 |
| 340 | PBGA 256 | 2.95 | 1.39 | 29.81 | 38.78 | 31.28 |
| 341 | PBGA 256 | 3.47 | 1.42 | 29.92 | 38.85 | 31.28 |
| 651" | PBGA313 | 4.1 | 1.58 | 29.64 | 31.86 | 30.54 |
| 652 | PBGA313 | 3.7 | 1.4 | 29.54 | 31.77 | 30.57 |
| 800 | SPBGA 352 | 2.81 | 1.09 | 28.87 | 31.28 | 30.03 |
| 801 | SPBGA 352 | 3.53 | 1.04 | 28.9 | 31.08 | 30.09 |
| 500 | OMPAC 352 | 4.46 | 1.5 | 29.61 | 32.29 | 30.9 |
| 501 | OMPAC 352 | 3.4 | 1.4 | 29.8 | 37.28 | 30.96 |

die edges and outer edges. Gull wings will have only one channel of daisy wiring that connects all the leads.

- JPL will require nearly 2,000 channels to perform complete electrical monitoring. The channels requirement is becoming one of the major limitations in increasing the number of PWBs assemblies for environmental exposure.
- For PBGA, Solder Mask Defined (SMD) were used to increase stand off and therefore reliability. The SMD has been used by Motorola, even though recently, they are optimizing use of NSMD (Non SMD) pad definition.
- For CBGA, NSMD configuration was used as recommended by IBM.

PWB AND PACKAGE INSPECTION

Packages and PWBs were inspected to document quality and reject those that are unacceptable. Ceramic BGAs were X-rayed prior to assembling to determine the level of solder voids, if any, and to distinguish these from those induced during manufacturing.

Planarity of packages was also measured. Planarity can contribute to the yield of surface mount manufacturing as well as long-term solder joint integrity. Package coplanarity is defined as the distance between the highest solder ball and the lowest solder ball. There is a direct correlation between coplanarity and package substrate, package size, and package thickness. Also, board planarity in assembly will contribute to the solder joint distortion level and will affect solder joint reliability with temperature cycling.

The 3-D Laser scanning equipment developed by View Engineering was used to determine planarity and ball diameter of each individual balls of all packages. Package warpage was also documented. Table 3 lists sample measurements of the maximum coplanarity and solder diameters of all packages for comparison. Each package will be tracked by its serial number and coplanarity results will be compared with manufacturing defect occurrence level to determine the level of correlation.

TEST VEHICLE ASSEMBLING

Celestica, an experienced BGA manufacturing facility as well as RIT with minimum experience in this area, will assemble the BGA test vehicles. Except for solder volume that is to be toggled, there are many manufacturing parameters that will be kept constant or are assumed to be constant, including reflow profile. Three solder levels, normal, low, and high, will be toggled with both PWB

types and I/O counts to fully characterize and define attributes of solder volume. Solder volume will be toggled for CBGA and at different levels for PBGA and QFP using optimum volume ranges for these packages.

Celestica assembled eight trial test vehicles to characterize thermal profile and optimize reflow process for both "300" and "600" I/O count test vehicles. After process optimization, two test vehicles were assembled and were X-rayed. Void contents were within acceptable ranges and they passed an electrical continuity test validation test. Power dissipation characteristics of 560 SPBGA with resistive die were measured. Solder joints were visually inspected and solder joints located at the edge of package were inspected using SEM.

Those solder joints inspected by SEM generally showed excellent fillet with smooth transition to PWB and balls for the case of CBGAs and with no signs of solder defects such as dewetting or insufficient solder. The test vehicles will be cross-sectioned to verify inspection results and to document solder joints' microstructure for reference. Since solder joints quality of trial test vehicles were acceptable, Celestica is now ready to assemble 170 test vehicles per the DoE test plan.

Two test vehicles were assembled at RIT and one was X-rayed and checked for continuity. This test vehicle is being evaluated for solder joint quality. RIT needs further work to optimize reflow processing. Once process is optimized, RIT will assemble about 30 test vehicles as defined in the DoE test matrix.

ENVIRONMENTAL TESTS

The present test program includes two thermal cycle profiles, and a combination of thermal and mechanical environmental exposure (Dynamic cycling). Power cycling will be performed using 560 SPBGA with AMD resistive die to better understand the behavior in a more realistic environment.

Thermal Cycling

The DOE plan details the number of assemblies that will be subjected to a specific thermal cycling profile (see Table 1). Most of assemblies will be subjected to the JPL thermal cycle and remaining will be subjected to a more severe military type cycle at Boeing and EMPF. Assemblies will be monitored during environmental testing.

The JPL cycle involves cycling between -30°C to 100°C with one and half hour duration. Dwell time at the maximum temperature will be 20 minutes to assure

completion of solder creep. Thermal cycling will be monitored continuously for electrical failure. JPL has recently generated extensive data on surface mount reliability of a variety of components including leadless chip carriers (LCCs), J-lead components, and gull wing components using this and several other thermal cycle profiles. This allows a direct comparison between BGA solder joint reliability and JPL's large SMT solder joint reliability data base.

The effects of an increase in maximum temperature and decrease in minimum temperature will be evaluated using a military type cycle, -55°C to 125°C. This cycle is the one generally used for qualification of military hardware, thereby covering Hughes' and Boeing's application requirements.

CURRENT AND FUTURE ACTIVITIES

Currently, the consortium is finalizing modifications required for the DoE test matrix manufacturing implementation based on the evaluation of the trial test vehicles assembled at Celestica and RIT. All test vehicles will be assembled per the DoE test matrix plan in late January '96. Environmental test procedures and types and intervals of data collection will be finalized by team members at a Workshop meeting. After inspection completion, all environmental testings are expected in February '96. The majority of environmental tests will be performed at JPL and the remaining at Boeing and EMPF. JPL has finalized acquisition of a new electrical monitoring system, thermal testing and inspection methodology. Continuous electrical monitoring, inspection by SEM and selective cross-sectioning of test vehicles will be performed as they are tested to failure.

Data collected will be analyzed and delivered in the following form:

- Weibull reliability plots using DoE matrix.
- Coffin-Manson relationship including results for increase in 1/0 and change in temperature range.
- Manufacturing defect and frequency for BGAs and fine pitch technology when different surface finishes are used.
- Correlation of manufacturing defect and package type and cycles to failure.
- Theoretical modeling and correlation to test results including thermal cycling and power cycling.

The output of this effort will be published in a suitable industrial guidelines document, providing a common point of reference and use between NASA/JPL and industry for this technology.

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